

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicant: Giulio-Giuseppe Marotta et al.

Title: ENHANCED PROTECTION FOR INPUT BUFFERS OF LOW-VOLTAGE FLASH MEMORIES

Docket No.: 303.698US2

Filed: September 29, 2003

Examiner: Don Le



Serial No.: 10/673,756

Due Date: August 17, 2004

Group Art Unit: 2819

Mail Stop Amendment

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

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☒ A Response (3 Pages).

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

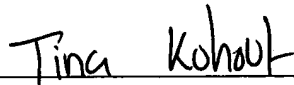
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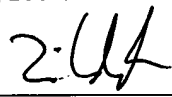
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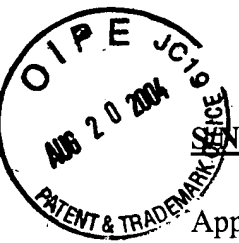
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Signature

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

(GENERAL)



SEN 10/673,756

PATENT

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Serial No.:	10/673,756	Group Art Unit:	2819
Filed:	September 29, 2003	Docket No.:	303.698US2
Title:	ENHANCED PROTECTION FOR INPUT BUFFERS OF LOW-VOLTAGE FLASH MEMORIES		

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REMARKS

This is in response to the Office Action mailed on May 17, 2004, and the references cited therewith.

No claims are amended, no claims are canceled, and no claims are added; as a result, claims 43-71 are now pending in this application.

Double Patenting Rejection

Claims 43-71 were rejected under the judicially created doctrine of double patenting over claims 1-43 of U.S. Patent No. 6,628,142. Applicants respectfully traverse this rejection.

The outstanding Office Action states that the conflicting claims contain similar elements, specifically an input node coupled to a buffer that is controlled by an inhibit signal. Applicant respectfully submits that the essential elements of the present application are not the same as the essential elements of U.S. Patent No. 6,628,142, and that the operation of the two devices is different, and results in different outcomes.

Independent claim 43 recites an input node connected to a pass transistor. The pass transistor is controlled by an inhibit signal to either interrupt or pass an input signal from the input node to an input signal node. The input signal node is either at the potential of the input signal, or if the pass transistor interrupts the input signal, then the input signal node biased to a predetermined voltage by bias circuit which switches on whenever the inhibit signal causes the pass transistor to interrupt the input signal. The inhibit signal is provided by control circuitry.